CLAIMS

What is claimed is:

1. A reference voltage generator comprising:

a first current source operative to generate a first current, the first current source having a first temperature coefficient;

an output current mirror operatively coupled to mirror the first current and to generate a second current in response to the first current;

an output device operative to provide a reference voltage in response to the second current; and

a shunt device, having a second temperature coefficient complementary to the first temperature coefficient, operatively coupled in parallel with the output device.

2. The reference voltage generator as set forth in Claim 1, wherein the first current source is a PMOS transistor coupled to apply a gate-source voltage difference on a first resistive element to generate a compensation current.

3. The reference voltage generator as set forth in Claim 1, wherein the shunt device is operative to restore the reference voltage in response to variations in the first current.

4. The reference voltage generator as set forth in Claim 1, wherein the shunt device is operative to restore the reference voltage in response to temperature-dependent variations in the first current.

5. The reference voltage generator as set forth in Claim 1, further comprising a compensation element operative to conduct a compensation current that varies in response to the first current, such that a one-to-one correspondence exists between the compensation current and the first current.

6. The reference voltage generator as set forth in Claim 5, further comprising a feedback element operative to conduct the compensation current such that the compensation current varies

inversely in response to the first current, such that an inverse one-to-one correspondence exists between the first current and the compensation current, and wherein the feedback element and the compensation element operate to restore the first current to a substantially constant first current.

7. The reference voltage generator as set forth in Claim 5, wherein the compensation element is a first resistive element.

8. The reference voltage generator as set forth in Claim 1, further comprising a feedback element operative to conduct a compensation current that varies *inversely* in response to the first current, such that a one-to-one correspondence exists between the compensation current and the first current.

9. The reference voltage generator as set forth in Claim 2, wherein the output device is a second resistive element coupled to be applied with the second current to generate the reference voltage.

10. The reference voltage generator as set forth in Claim 9, wherein the shunt device is an NMOS transistor connected to the second resistive element in parallel to compensate for a variation of the gate-source voltage difference.

11. A method for generating a reference voltage, comprising:
generating a first current having a first temperature coefficient;
mirroring the first current and generating a second current in response to the first current;
providing a reference voltage in response to the second current; and
shunting a current having a second temperature coefficient complementary to the first temperature coefficient in parallel with the second current.

12. The method for generating a reference voltage as set forth in Claim 11, wherein the generating of a first current having a first temperature coefficient includes:
applying a first gate-source voltage difference to a PMOS transistor; and

applying the first gate-source voltage difference to a first resistive element.

13. The method for generating a reference voltage as set forth in Claim 11, wherein the shunting of a current having a second temperature coefficient complementary to the first temperature coefficient in parallel with the second current further includes restoring the reference voltage in response to variations in the first current.

14. The method for generating a reference voltage as set forth in Claim 11, wherein the shunting of a current having a second temperature coefficient complementary to the first temperature coefficient in parallel with the second current further includes restoring the reference voltage in response to temperature-dependent variations in the first current.

15. The method for generating a reference voltage as set forth in Claim 11, wherein the generating of a first current having a first temperature coefficient includes:

applying a first gate-source voltage difference to a first resistive element; and

conducting a compensation current that varies in response to the first current, such that a one-to-one correspondence exists between the compensation current and the first current.

16. The method for generating a reference voltage as set forth in Claim 15, further comprising conducting the compensation current such that the compensation current varies inversely in response to the first current, such that an inverse one-to-one correspondence exists between the first current and the compensation current, and wherein a feedback element and a compensation element operate to restore the first current to a substantially constant first current.

17. The method for generating a reference voltage as set forth in Claim 11, further comprising conducting a compensation current that varies inversely in response to the first current, such that a correspondence exists between the compensation current and the first current.

18. The method for generating a reference voltage as set forth in Claim 12, further comprising applying the reference voltage to a second resistive element.

19. The method for generating a reference voltage as set forth in Claim 18, further comprising compensating a variation of the gate-source voltage difference by applying the reference voltage to an NMOS transistor connected to the second resistive element in parallel.

20. A reference voltage generator, comprising:

a first resistive element;

a PMOS transistor coupled to apply a gate-source voltage difference on the first resistive element to generate a first current;

a current mirror for mirroring the first current to generate a second current;

a second resistive element coupled to be applied with the second current to thereby generate a reference voltage; and

an NMOS transistor connected to the second resistive element in parallel for compensating a variation of the gate-source voltage difference.

21. The reference voltage generator as set forth in Claim 20, further comprising a capacitive element connected to the second resistive element in parallel.